CLAIMS

SUB C6

1. A transistor having at least one, substantially one-dimensional, elongate conducting means provided by at least a first semiconductor substantially surrounded by a second semiconductor and extending between source and drain electrodes, and in which there is provided at least one further electrode in a region of the elongate conducting means, the elongate conducting means being provided in a groove within the second semiconductor, said groove being orientated such that at least one wall of the groove is a, substantially planar, surface, roughly parallel to a crystal plane on which the growth rate of the first semiconductor is substantially zero.

2. A transistor according to claim 1 wherein the groove is provided by an intersection of two walls, each wall being a substantially planar, surface, roughly parallel to a crystal plane on which the growth rate of the first semiconductor is substantially zero.

3. A transistor according to claim 2 wherein the first semiconductor is provided in a region of the intersection.

4. A transistor according to ~~any one of claims 1 to 3~~ claim 1 comprising a groove formed into a substrate having a region of the second semiconductor provided on the sides of the grooves lining the groove.

5. A transistor according to claim 4 wherein the first semiconductor and the substrate are substantially the same material.

SUB C7 6. A transistor according to ~~any one of the preceding claims~~ claim 1 wherein the conducting means comprises an elongate region of the first

semiconductor in a bottom region of the second semiconductor, that is in a bottom region of the lined groove, or in a bottom region of the groove.

7. A transistor according to ~~any one of the preceding claims~~ claim 1 wherein the groove is provided within a top region of a mesa structure.

8. A transistor according to ~~any one of the preceding claims~~ claim 1 wherein there is provided more than one conducting means.

9. A transistor according to ~~any one of the preceding claims~~ claim 1 wherein a quantum dot is provided along a region of the conducting means.

10. A transistor according to claim 9 wherein the at least one further electrode is adapted, in use, to provide the confinement to provide the quantum dot.

11. A transistor according to claim 9 ~~or 10~~ wherein there are provided a plurality of quantum dots along the conducting means.

12. A transistor according to ~~any one of the preceding claims~~ claim 1 wherein the electrode or electrodes are arranged to provided confinement in a third dimension for charge carriers within the conducting means, in which hard confinement in two dimensions holds charge carriers within the conducting means.

13. A transistor according to ~~any one of the preceding claims~~ claim 1 wherein the electrode or electrodes are substantially transverse to the conducting means.

14. A transistor according to ~~any one of the preceding claims~~ claim 1 wherein the electrode or electrodes are, in use, capable of causing a peak within the energy bands of the first semiconductor of the conducting means.

15. A transistor according to ~~any preceding claim~~ claim 1 wherein a portion of the conducting means has a crescent shaped cross section.

16. A transistor according to ~~any one of the preceding claims~~ claim 1 wherein the first semiconductor is gallium arsenide (GaAs).

17. A transistor according to ~~any one of the preceding claims~~ claim 1 wherein the second semiconductor is aluminium gallium arsenide (AlGaAs).

18. A transistor according to ~~any one of the preceding claims~~ claim 1 which is a single electron transistor.

19. A method of providing a transistor comprising providing a substantially one-dimensional elongate conducting means by providing a first semiconductor substantially surrounded by a second semiconductor material, the elongate conducting means being provided by creating a groove of second semiconductor such that at least one wall of the groove is a substantially planer surface roughly parallel to a crystal plane on which the growth rate of the first semiconductor is substantially zero and subsequently providing the first semiconductor in the groove, providing a source electrode at a first end region of the conducting means and a drain electrode at a second end region of the conducting means, and providing at least one further gate electrode in a region of the conducting means.

20. A method according to claim 19 comprising providing the groove by performing an anisotropic etch.

21. A method according to claim 19 ~~or 20~~ wherein the groove is provided in an n^+ epilayer grown onto a substrate.

22. A method according to claim 21 wherein the substrate and first semiconductor are substantially the same material.

23. A method according to claim 21 ~~or 22~~ wherein the groove is provided in a p^- doped region provided in a top region of the n^+ epilayer.

24. A method according to ~~any one of claims 19 to 23~~ claim 19 wherein the groove of second semiconductor is provided by lining a groove with second semiconductor.

25. A method according to claim 24 wherein the first semiconductor is grown in a bottom region of the lined groove.

26. A method according to ~~any one of claims 19 to 25~~ claim 19 wherein the first semiconductor is surrounded by the second semiconductor by provision of a layer of second semiconductor once the first semiconductor has been provided.

27. A method according to ~~any one of claims 19 to 26~~ claim 19 wherein the first material is GaAs.

28. A method according to ~~any one of claims 19 to 27~~ claim 19 wherein the second semiconductor is AlGaAs.

29. A method according to ~~any one of claims 19 to 28~~ Claim 19 wherein the groove is arranged such that the walls of the groove lies substantially along the (111) planes of the semiconductor.

30. A method according to ~~any one of claims 19 to 29~~ Claim 19 wherein the groove in the substrate is formed slightly off axis from the planes of the semiconductor.

31. A method according to claim 30 wherein quantum dots are provided along the conducting means in the vicinity of stops caused due to thickness variations of the conducting means due to the off axis groove.

32. A method according to ~~any one of claims 19 to 31~~ Claim 19 wherein the transistor is a single electron transistor (SET).